## What is claimed is:

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- 1 1. An apparatus for data input comprising:
- a sensing circuit for a plurality of keys, outputting an interruption signal and a corresponding group of data bits when one of the keys is pressed;
  - a shift register circuit receiving a strobe signal, a clock signal and the group of data bits in parallel from the sensing circuit when the strobe signal is asserted, and serially outputting the group of data bits in synchronization with the clock signal; and
  - a microcontroller receiving the interruption signal, outputting the strobe signal and clock signal when the interruption signal is asserted, and serially receiving the group of data bits from the shift register circuit to identify the key being pressed.
- 1 The apparatus as claimed in claim 1, wherein the keys are implemented with a plurality of switches, 2 sensing circuit further comprises a plurality of first 3 4 impedances and a second impedance, each of the switches has a first and second end respectively coupled to a first end 5 of one of the first impedances and to receive a second 6 voltage level, the second impedance has a first and second 7 end respectively coupled to receive a first voltage level 8 9 and second ends of the first impedances.

- 1 3. The apparatus as claimed in claim 2, wherein the 2 first and second voltage level are respectively a power
- 3 supply and ground voltage.
- 1 4. The apparatus as claimed in claim 1, wherein the 2 shift register circuit further comprises:
- a plurality of logic gates, each having input terminals
  coupled to receive the strobe signal and one of
  the data bits from the sensing circuit, and
  outputting the received data bit when the strobe
  signal is asserted; and
- a plurality of flip-flops, each having a first input 8 terminal receiving the data bit from one of the 9 logic gates, a second input terminal and a third 10 input terminal receiving the clock signal, and an 11 output terminal coupled to the second 12 terminal of an adjacent flip-flop and outputting 13 14 the data bit received by the first 15 terminal.
  - The apparatus as claimed in claim 1, wherein the interruption signal is asserted by a low logic voltage level.
  - 1 6. The apparatus as claimed in claim 1, wherein the 2 strobe signal is asserted by a low logic voltage level.
  - 7. The apparatus as claimed in claim 1, wherein the group of data bits comprises eight data bits.
  - 1 8. An apparatus for data input comprising:

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- a sensing circuit for a plurality of keys, outputting
  an interruption signal and a corresponding group
  of data bits when one of the keys is pressed;
  - a control circuit coupled to the sensing circuit outputting a strobe signal and clock signal when the interruption signal is asserted;
- a shift register circuit coupled to the sensing circuit
  and control circuit, receiving the strobe signal,
  the clock signal and the group of data bits in
  parallel from the sensing circuit when the strobe
  signal is asserted, and serially outputting the
  group of data bits in synchronization with the
  clock signal; and
- an identifying circuit coupled to the shift register circuit and serially receiving the group of data bits from the shift register circuit to identify the key being pressed.
  - 9. The apparatus as claimed in claim 8, wherein the control and identifying circuit are disposed in a microcontroller.
  - 1 10. The apparatus as claimed in claim 8, wherein the 2 interruption signal is asserted by a low logic voltage 3 level.
  - 1 11. The apparatus as claimed in claim 8, wherein the 2 strobe signal is asserted by a low logic voltage level.
  - 1 12. The apparatus as claimed in claim 8, wherein the 2 group of data bits comprises eight data bits.

1 A method for key detection in an apparatus for 2 data input comprising a sensing circuit for a plurality of 3 keys, a shift register, and a microcontroller, the method comprising the steps of: 4 5 outputting by the sensing circuit a group of data bits corresponding to one of the keys being pressed; 6 receiving the group of data bits from the sensing 7 circuit in parallel and serially outputting the 8 received group of data bits by the shift register 9 10 circuit; and serially receiving the group of data bits from the 11 shift register circuit to identify the key being 12 13 pressed. The method as claimed in claim 13, wherein the 1 group of data bits comprises eight data bits. 2 1 An apparatus for data input comprising: 2 a switch circuit having a plurality of keys and forming an equivalent RC circuit corresponding to one of 3 the keys being pressed; 4 an oscillator generating a sinusoidal wave signal with 5 a frequency corresponding to the equivalent RC 6 7 circuit formed by the switch circuit when the key 8 is pressed; 9 a square wave generator receiving the sinusoidal wave 10 from the oscillator to generating a corresponding square wave signal; and 11 a processor identifying the key being pressed according 12

to the square wave.

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- 1 16. The apparatus as claimed in claim 15, wherein the
- 2 equivalent RC circuit has an RC constant.
- 1 17. The apparatus as claimed in claim 16, wherein the
- 2 RC constants of the equivalent RC circuits corresponding to
- 3 the pressed keys are different from each other.
- 1 18. The apparatus as claimed in claim 15, wherein the
- 2 frequency of the sinusoidal wave signal corresponds to an RC
- 3 constant of the equivalent RC circuit.
- 1 19. The apparatus as claimed in claim 15, wherein a
- 2 frequency of the square wave signal corresponds to that of
- 3 the sinusoidal wave signal.
- 1 20. The apparatus as claimed in claim 19, wherein a
- 2 frequency of the square wave signal equals that of the
- 3 sinusoidal wave signal.
- 1 21. The apparatus as claimed in claim 15, wherein each
- 2 of the keys is a switch coupled to an output terminal of the
- 3 oscillator.
- 1 22. The apparatus as claimed in claim 15, wherein the
- 2 switch circuit further comprises a plurality of resistors
- 3 coupled between the keys and the oscillator.
- 1 23. The apparatus as claimed in claim 22, wherein the
- 2 oscillator comprises an operational amplifier with a
- 3 negative input terminal coupled to the resistors.

- 1 24. The apparatus as claimed in claim 22, wherein the
- 2 switch circuit further comprises a capacitor coupled between
- 3 the resistors and a ground.
- 1 25. The apparatus as claimed in claim 15, wherein the 2 oscillator further comprises:
- an operational amplifier having a negative input
- 4 terminal and output terminal coupled to the
- 5 switch circuit;
- 6 a first resistor coupled between a ground and a
- 7 positive input terminal of the operational
- 8 amplifier; and
- 9 a second resistor coupled between the output terminal
- and positive input terminal of the operational
- 11 amplifier.
  - 1 26. The apparatus as claimed in claim 25, wherein the
  - 2 switch circuit further comprises a plurality of resistors
  - 3 and a capacitor, each of the resistors is coupled between
  - 4 the negative input terminal of the operational amplifier and
  - 5 a first end of one of the keys, the capacitor is coupled
  - 6 between the ground and the negative input terminal of the
  - 7 operational amplifier, and second ends of the keys are
  - 8 commonly coupled to the output terminal of the operational
  - 9 amplifier.
  - 1 27. A method for key detection in an apparatus for
  - 2 data input comprising a switch circuit having a plurality of
  - 3 keys, the method comprising the steps of:

- 4 forming an equivalent RC circuit corresponding to one
- of the keys being pressed;
- 6 generating a sinusoidal wave signal with a frequency
- 7 corresponding to the equivalent RC circuit;
- 8 generating a square wave signal corresponding to the
- 9 sinusoidal wave signal; and
- 10 identifying the key being pressed according to the
- 11 square wave signal.
  - 1 28. The method as claimed in claim 27, wherein the
  - 2 switch circuit further comprises a plurality of resistors
  - 3 and a capacitor, one of the resistors corresponding to the
  - 4 pressed key is selected to form the equivalent RC circuit.
  - 1 29. The method as claimed in claim 28, wherein the
  - 2 equivalent RC circuit has an RC constant determined by a
  - 3 product of a capacitance of the capacitor and a resistance
  - 4 of the resistor.
  - 1 30. The method as claimed in claim 27, wherein RC
  - 2 constants of the equivalent RC circuits corresponding to the
  - 3 pressed keys are different from each other.
  - 1 31. The method as claimed in claim 30, wherein the
  - 2 frequency of the sinusoidal wave signal corresponds to the
  - 3 RC constant of the equivalent RC circuit.
  - 1 32. The method as claimed in claim 31, wherein a
  - 2 frequency of the square wave signal corresponds to that of
  - 3 the sinusoidal wave signal.

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- 1 33. The method as claimed in claim 32, wherein a
- 2 frequency of the square wave signal equals that of the
- 3 sinusoidal wave signal.